WHAT IS CLAIMED IS:

1. A multi-bit phase change memory cell, comprising:

a stack of a plurality of conductive layers and a plurality of phase change material layers, each of the phase change material layers disposed between a corresponding pair of conductive layers and having electrical resistances that are different from one another.

2. The multi-bit phase change memory cell of claim 1, the plurality of conductive layers including a first outer conductive layer disposed at one side of the memory cell and a second outer conductive layer disposed at a side opposite to the one side of the memory cell, the electrical resistance of each of the plurality of phase change material layers increasing along a direction from the first outer conductive layer to the second outer conductive layer.

3. The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have the same resistivity.

4. The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have a different phase transition temperature.

5. The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have the same phase transition temperature.

6. The multi-bit phase change memory cell of claim 3, wherein each of the plurality of phase change material layers have dimensions that are different from one another.

7. The multi-bit phase change memory cell of claim 1, the plurality of conductive layers including a plurality of intermediate conductive layers disposed between the first and second outer conductive layers, each of the intermediate conductive layers having the same dimensions as an adjacent phase change material layer.

8. The multi-bit phase change memory cell of claim 1, further comprising a dielectric layer formed between the first outer electrode and the second outer electrode and along sides of at least one other conductive layer and a phase change material layer disposed directly adjacent to the at least one other conductive layer.

9. The multi-bit phase change memory cell of claim 1, wherein the phase change material layers are made of the same material.

10. The multi-bit phase change memory cell of claim 1, wherein each of the phase change material layers are made of a different material.

11. The multi-bit phase change memory cell of claim 1, wherein the phase change material layers are made of $Ge_2Sb_2Te_5$.

12. The multi-bit phase change memory cell of claim 1, wherein the plurality of conductive layers are made of at least one of TiN, W, TiW, Ta, TaN, Ti, Al, Cu, and Pt.

13. The multi-bit phase change memory cell of claim 1, wherein the number of phase change material layers is equal to 2^n, where n is the number of bits stored in the memory cell.

14. A method of forming a multi-bit phase change memory cell, comprising:

forming a stack of a plurality of phase change material layers and a plurality of conductive layers, each of the phase change material layers disposed between a corresponding pair of conductive layers and having electrical resistances that are different from one another.

15. The method of claim 14, wherein each of the phase change material layers have a different phase transition temperature.

16. The method of claim 14, wherein the step of forming a plurality of conductive layers includes forming a first outer conductive layer, a second outer conductive layer opposite the first outer conductive layer, and a plurality of intermediate conductive layers disposed between the first outer conductive layer and the second outer conductive layer, the method further comprising:

forming a dielectric layer between the first outer conductive layer and the second outer conductive layer and at sides of the plurality of intermediate conductive layers and the plurality of phase change material layers.

17. The method of claim 16, wherein the step of forming a dielectric layer comprises forming dielectric

spacers at sides of each of the plurality of phase change material layers.

18. The method of claim 17, wherein the step of forming a dielectric layer comprises:

forming a mask over the first outer conductive layer;

etching the first outer conductive layer and a phase change material layer directly below the first outer conductive layer using the mask;

forming first dielectric spacers on sides of the mask, the first outer conductive layer and the phase change material layer directly below the first outer conductive layer;

etching at least one intermediate conductive layer and a phase change material layer directly below the at least one intermediate layer using the mask and first dielectric spacers as an etchant mask; and

forming second dielectric spacers on sides of the first dielectric spacers, the at least one intermediate conductive layer and the phase change material layer below the at least one intermediate conductive layer.

19. The method of claim 14, wherein the step of forming a stack comprises forming 2^n layers of phase change

material layers, where n is the number of bits to be stored in the memory cell.

20. The method of claim 14, wherein the plurality of phase change material layers are made of $Ge_2Sb_2Te_5$.

21. The method of claim 14, wherein the plurality of conductive layers are made of at least one of TiN, W, TiW, Ta, TaN, Ti, Al, Cu, and Pt.

22. A multi-bit phase change memory, comprising:

an array of multi-bit phase change memory cells, each of the multi-bit phase change memory cells comprising:

a stack of a plurality of conductive layers and a plurality of phase change material layers, each of the phase change material layers disposed between a corresponding pair of conductive layers and having electrical resistances that are different from one another;

a programming circuit that writes data to the array of multi-bit phase change memory cells; and

a sensing circuit that reads out data from the array of multi-bit phase change memory cells.

23. The method of claim 22, wherein the plurality of phase change material layers are made of $Ge_2Sb_2Te_5$.

24. A method of programming a multi-bit phase change memory cell, comprising:

phase changing at least one phase change material layer of the multi-bit phase change memory cell to change the overall resistance of the multi-bit phase change memory cell to one of 2^n number of resistances, where n is the number of bits stored in the memory cell.

25. The method of claim 24, wherein the step of phase changing comprises a step of inputting a current pulse to the at least one phase change material layer.